## REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

The drawings have been objected on the grounds of not illustrating the claimed first and second structure data. While this intermediary language has been removed from the claims in favor of direct use of the first and second endian byte order, the first and second structure data are shown in Fig. 13 (elements 10b and 20b) and in Fig. 14 (elements 10c and 20c).

Claims 9-11, 16-19, and 24-27 have been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner asserts that the recitations in claim 9 (and similar recitations in claims 16 and 19) of "wherein said memory stores structure data to be accessed by said first-endian processor and said second-endian processor, wherein the structure data includes first structure data and second structure data" and "including the second structure data in which data that is smaller than the basic word length is defined to be in an order that is reverse of the defined order in the first structure data" are not disclosed in the Specification of the present application. This rejection is traversed and is inapplicable to the claims as amended.

Support for the elements of claim 9 is shown below in bold. These passages also support the similar recitations in claims 16 and 19.

9. A data sharing apparatus comprising:

a data bus **("D-bus" in Fig. 7)** having a data width;

a memory **(30 in Fig. 7)** which stores data according to a first-endian byte order **(e.g., page 11, line 31 to page 12, line 19)**;

a first-endian processor logically connected to said ~~memory in a~~memory in the first-endian byte order via said data bus **(e.g., page 11, line 31 to page 12, line 7)**, wherein said first-endian processor executes a first program that utilizes the first endian byte order in which data is defined as being in a defined order **(e.g., page 16, lines 23-25, and the order shown in 10b of Fig. 13)**;

a second-endian processor logically connected to said memory in the first-endian byte order

via said data bus **(e.g., page 12, lines 7-19)**, wherein said second-endian processor executes a second program that utilizes a second endian byte order in which data that is smaller than the basic word length is defined to be in an order that is reverse of the defined order of the first endian byte order **(e.g., page 16, lines 25-30, and the order shown in 20b of Fig. 13)**; and

an address conversion unit **(e.g., 21 in Fig. 7)** operable:

(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data **(e.g., the "B(8bits) row in Fig. 8)**;

(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data **(e.g., the "hw(16bits) row in Fig. 8)**; and

(iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus **(e.g., the "w(32bits) row of Fig. 8)**.

In view of the above, it is submitted that the claimed inventions are adequately described in the Specification as filed. Accordingly, it is submitted that claims 9-11, 16-19, and 24-27 are in compliance with 35 U.S.C. 112, first paragraph

Claims 16-18, and 24-25 have been rejected under 35 U.S.C. 112, second paragraph as being indefinite due to lack of antecedent basis for the language "the structure data" in claim 16. Claim 16 as amended no longer includes this language. Accordingly, it is submitted that claims 16-18, and 24-25 are in compliance with 35 U.S.C. 112, second paragraph.

In view of the above, it is submitted that claims 9-11, 16-19, and 24-27 are allowable over the prior art of record. It is therefore submitted that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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